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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/714,801	11/17/2003	Yun-Ho Choi	SAM-0486	2965

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EXAMINER	
GRAYBILL, DAVID E	
ART UNIT	PAPER NUMBER
2822	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/714,801	CHOI ET AL.	
	Examiner	Art Unit	
	David E. Graybill	2822	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 November 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-5,7,9,11-15,17 and 19* is/are pending in the application.

4a) Of the above claim(s) *9,11-15,17 and 19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-5 and 7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Newly submitted claim 19 is directed to an invention that is independent or distinct from the invention originally claimed for the following reasons: It is directed to a species non-elected in the response filed on 12-18-6.

Since applicant has received an action on the merits for the originally presented invention, this invention has been constructively elected by original presentation for prosecution on the merits. Accordingly, claim 19 is withdrawn from consideration as being directed to a non-elected invention. See 37 CFR 1.142(b) and MPEP § 821.03.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the

contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over the combination of Corisis (6607937) and Chang (20020153599).

At column 1, lines 12-17; column 4, line 28 to column 5, line 25; and column 5, line 60 to column 6, line 37, Corisis discloses the following:

Re claim 1: A multi-chip package comprising: a first semiconductor chip 220a which shows good results when tested for reliability after being assembled at a package level; at least one second semiconductor chip 220b which is in a wafer level configuration and is stacked on the first semiconductor chip via inherent stacking means "the upper packaged device 220b can be attached to the lower packaged device 220a", wherein a back surface of the first semiconductor chip faces a back surface of the second semiconductor chip; a first connecting unit 243a attached to a surface opposite the back surface of the first semiconductor chip; and a second connecting unit 243b attached to a surface opposite the back surface of the second semiconductor chip, wherein the first connecting unit is different

from the second connecting unit, and the first semiconductor chip includes a packaged "memory".

To further clarify, Corisis discloses that the back surface abuts the back surface because Corisis discloses that the back surface touches (is in contact with (at least indirectly)) along a border with the back surface. To further afford applicant the benefit of compact prosecution, it is noted that there is no support in the original disclosure for the scope of the term abuts to be limited to wherein the back surface is in direct contact with the back surface because the original disclosure discloses adhesive between the surfaces, and such a limitation is not otherwise originally disclosed.

However, Corisis does not appear to explicitly disclose the following:

Re claim 1: for electrically connecting the first semiconductor chip to an external system; for electrically connecting the second semiconductor chip to the external system.

Nonetheless, the language "for electrically connecting the first semiconductor chip to an external system," and, "for electrically connecting the second semiconductor chip to the external system" are statements of intended use of the connecting units that do not appear to result in a structural difference between the claimed units and the units of Corisis. Further, because the units of Corisis appear to have the same structure as the claimed units, they appear to be capable of being used for the intended

uses, and the statements of intended use do not patentably distinguish the claimed units from the units of Corisis. The manner in which a product operates is not germane to the issue of patentability of the product; Ex parte Wikdahl 10 USPQ 2d 1546, 1548 (BPAI 1989); Ex parte McCullough 7 USPQ 2d 1889, 1891 (BPAI 1988); In re Finsterwalder 168 USPQ 530 (CCPA 1971); In re Casey 152 USPQ 235, 238 (CCPA 1967). Also, "Expressions relating the apparatus to contents thereof during an intended operation are of no significance in determining patentability of the apparatus claim."; Ex parte Thibault, 164 USPQ 666, 667 (Bd. App. 1969). And, "Inclusion of material or article worked upon by a structure being claimed does not impart patentability to the claims."; In re Young, 25 USPQ 69 (CCPA 1935) (as restated in In re Otto, 136 USPQ 458, 459 (CCPA 1963)). And, claims directed to product must be distinguished from the prior art in terms of structure rather than function. In re Danley, 120 USPQ 528, 531 (CCPA 1959). "Apparatus claims cover what a device is, not what a device does [or is intended to do]." Hewlett-Packard Co. v. Bausch & Lomb Inc., 15 USPQ2d 1525, 1528 (Fed. Cir. 1990).

However, Corisis does not appear to explicitly disclose that the first semiconductor chip includes a flash memory.

Nonetheless, at paragraph 9, Chang discloses that a first semiconductor chip 21 includes a flash memory. Furthermore, it would have

been obvious to combine this disclosure of Chang with the disclosure of Corisis because it would facilitate provision of the first semiconductor chip which includes a memory of Corisis.

Claims 2, 4, 5 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Corisis and Chang as applied to claim 1, and further in combination with Saeki (20030122237).

As cited supra, Corisis discloses the following:

Re claim 2: The multi-chip package of claim 1, further comprising a printed circuit board 230 for the multi-chip package, which includes bonding pads 231a, 231b to which the first connecting unit and the second connecting unit are connected.

However, Corisis and Chang do not appear to explicitly disclose the following:

Re claim 2: pins for connecting the bonding pads to the external system.

Nevertheless, at paragraphs 22, 25, 43 and 49, Saeki discloses pins 33-35 for connecting the bonding pads 32 to the external system "the printed wiring board or the like". Furthermore, it would have been obvious to combine this disclosure of Saeki with the disclosure of Corisis and Chang because it would facilitate external electrical connection.

However, in the particular embodiment for which Corisis is relied on, the combination of Corisis and Chang does not appear to explicitly disclose the following:

Re claim 3: The multi-chip package of claim 2, further comprising a molding compound for fastening the first and second semiconductor chips and protecting the first and second semiconductor chips from the external environment.

Re claim 4: The multi-chip package of claim 3, wherein the stacking means are an adhesive.

Regardless, as cited, in another embodiment Corisis discloses a molding compound 423c inherently for fastening the first and second semiconductor chips and protecting the first and second semiconductor chips from the external environment, wherein the stacking means are an "adhesive". In addition, it would have been obvious to combine these disclosures of Corisis because it would protect the first and second chips from the external environment and facilitate stacking.

Also, the combination of Corisis and Chang does not appear to explicitly disclose the following:

Re claim 5: The multi-chip package of claim 4, wherein a package type of the first semiconductor chip is a Wafer-Level Chip Size Package (W-CSP).

Re claim 7: The multi-chip package of claim 5, wherein a package type of the printed circuit board is a Ball Grid Array (BGA).

Notwithstanding, as cited, Saeki discloses wherein a package type of the first semiconductor chip is a Wafer-Level Chip Size Package (W-CSP) and a package type of the printed circuit board is a Ball Grid Array (BGA) (34, 35 illustrated in Fig. 2). Moreover, it would have been obvious to combine this disclosure of Seki with the disclosure of Corisis and Chang because it would facilitate provision of the first chip of Corisis, minimize package size and facilitate external electrical connection.

Applicant's amendment and remarks filed 11-8-7 have been fully considered, are treated supra, and are further addressed infra.

Applicant's request for reconsideration of the withdrawal of claims 2-5 and 7 is deemed persuasive. Therefore, the withdrawal of claims 2-5 and 7 has been withdrawn and claims 2-5 and 7 are examined on the merits.

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will

expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

For information on the status of this application applicant should check PAIR: Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alternatively, applicant may contact the File Information Unit at (703) 308-2733. Telephone status inquiries should not be directed to the examiner. See MPEP 1730VIC, MPEP 203.08 and MPEP 102.

Any other telephone inquiry concerning this communication or earlier communications from the examiner should be directed to David E. Graybill at (571) 272-1930. Regular office hours: Monday through Friday, 8:30 a.m. to 6:00 p.m.
The fax phone number for group 2800 is (571) 273-8300.

David E. Graybill
Primary Examiner
Art Unit 2822

D.G.
18-Jan-08